

Optimization of Edge Termination Techniques for β-Ga₂O₃ Schottky Rectifiers

Ribhu Sharma, 61,z Erin E. Patrick, M. E. Law, F. Ren, 3,** and S. J. Pearton 61,**

To realize the potential of Gallium oxide (Ga_2O_3) Schottky rectifiers fabricated for high voltage and fast switching applications, various edge termination techniques to maximize the breakdown voltage (V_{br}) are studied and examined via simulations using the FLOODS/FLOOPS TCAD simulator. The simulated Schottky rectifiers consist of a Si-doped $(n=1.0\times10^{15}-1.3\times10^{17}~cm^{-3})$ β -Ga₂O₃ epitaxial layer grown on Sn-doped $(n=4.8\times10^{18}~cm^{-3})$ Ga₂O₃ substrates. The optimization of field plate geometry for Schottky barrier diodes (SBD) was investigated using the device breakdown characteristics as the figure-of-merit. Various field plate dielectrics (SiO₂, SiN_x, Al₂O₃, and HfO₂) were explored while the field plate structure was concurrently varied to obtain a normalized breakdown field (V_{Nbr}) of \sim 3 for a step (graduated form) dielectric with Al₂O₃ as the dielectric. Edge termination via the formation of resistive areas at the anode contact periphery via ion (argon) implantation was also examined for the SBDs since other edge termination techniques are ineffective due to lack of p-type doping in Ga₂O₃. The configuration of the implanted region was investigated and a V_{Nbr} of over 5 was achieved for diodes with an unbounded resistive region and an implantation depth of 50–100 nm

© The Author(s) 2019. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0141912jss]

Manuscript submitted October 14, 2019; revised manuscript received November 19, 2019. Published December 2, 2019.

The need for new and improved high-performance power switching electronics has emerged due to the recent progress of power electronics, automotive electronics, grid-scale energy storage, industrial control, and military systems. 1-8 Over the past few decades wide bandgap materials like GaN, SiC and Ga2O3 have been of interest to fulfill the requirements of electronic switching devices. Currently, state of the art devices have been fabricated from SiC and GaN, with GaN finding applications in fast-charging of home electronics,9 while SiC is commercialized for automotive charging applications. However, because of the larger bandgap of Ga_2O_3 ($E_g = 4.5-5.0$ eV), devices made on this material would have an advantage in terms of higher switching efficiency. The large bandgap translates to a high theoretical critical field strength (~8 MV/cm), and a high Baliga's figure-of-merit (BFOM), about 4-7 times that of SiC and leads to low conduction losses at a lower cost (represented by Huang's chip manufacturing FOM or HCAFOM) in comparison to 4H-SiC diodes. Furthermore, recent advancements in the growth techniques of high-quality Ga₂O₃ substrates have made large, inexpensive substrates available using traditional growth techniques. In addition, high-quality epitaxial layers have also been grown using metalorganic-chemical vapor deposition (MOCVD), hydride vaper phase epitaxy (HVPE), and molecular beam epitaxy (MBE). 10-16 High temperature operability is also possible due to the large bandgap; however, the low thermal conductivity is an issue with gallium oxide. Furthermore, additional limitations include the absence of p-type doping and the low electron mobility, which have sparked a lot of debate about the suitability of this material.

Using dopants like Si, Sn, and Ge, a wide range of electron densities $(10^{15} \text{ to } 10^{19} \text{ cm}^{-3})$ has been demonstrated. Despite the various technological limitations of Ga_2O_3 , the excellent breakdown characteristics make β - Ga_2O_3 Schottky barrier diodes ideal for low loss, high-voltage switching, and high-power applications. Over the past few decades, GaN and SiC devices have been developed to maximize the breakdown voltage $(V_{br})^{17-25}$ by using edge termination techniques like field plate structures, highly resistive areas by ion implantation, guard rings, and mesas. The need for efficient edge termination arises because high electric fields are created near the contact edges as the reverse voltage is increased, which causes irreversible anode degradation. A lot of attention has been given to high current β - Ga_2O_3 Schottky rectifiers with focus on achieving high reverse breakdown characteristics and

low on-state resistance (RON);^{26–29} however, edge termination has not been fully developed. The difficulty in implementing p-type doping has made it challenging to utilize edge termination techniques such as guard rings, or junction termination extensions, making field plate structures and ion-implanted regions near the contact edges the only available options.

A high \tilde{V}_{br} of over 2300V²⁷ has been reported for vertical large area field-plated β-Ga₂O₃ Schottky diodes fabricated on a 20 μm thick, very lightly doped (n = 2×10^{15} cm⁻³) epitaxial layer grown on a highly doped (n = $3.6 \times 10^{18} \text{ cm}^{-3}$) β -Ga₂O₃ substrate. Field-plated lateral β-Ga₂O₃ Schottky diodes³⁰ have shown a higher breakdown voltage of over 3000 V while also demonstrating devices with very high DC power FOM of 370-500 MW/cm². Progress on optimizing edge termination techniques for Ga₂O₃ rectifiers by Lin et al.,³¹ demonstrated the improvement in V_{br} by using N++ ion-implanted guard rings. Theoretical studies have predicted nitrogen atoms to be deep acceptors,³² with the nitrogen impurities having acceptor transition levels of 1.3eV above the conduction band maximum.³³ Various dielectric materials have been studied for field plated Ga2O3 diodes via simulation and initial reports³⁴ suggest some good candidates in Al₂O₃ and HfO₂ as the dielectric. Furthermore, edge termination via Ar ion implantation has also been studied for vertical Au/Ni/β-Ga₂O₃ Schottky barrier diodes³⁵ where the area near the contact edges has been implanted to create highly resistive regions, which helps in diminishing field crowding near the contact edge. Similar to nitrogen ions as stated earlier, ion implantation creates defects in the materials that increases the deep acceptor trap concentration causing compensation in the intrinsic n-type doped material.

In this paper, a comprehensive analysis of various edge termination structures and techniques is performed via simulations to test the effects of dimensionality, dielectric materials, structural variations and trap concentrations on the breakdown voltage. Schottky rectifiers fabricated by Carey et al. are considered as the basic device structure 36 with $\rm SiO_2, SiN_x, Al_2O_3,$ and $\rm HfO_2$ as the dielectrics, while the study by Gao et al. 35 is used as reference and validation for the Ar ion-implanted edge termination analysis.

Methods

The FLOODS TCAD simulator self-consistently solves the partial differential equations governing the physics of our model. The Florida Object Oriented Device and Process simulator (FLOODS/FLOOPS) is a partial differential equation (PDE) solver, written as an

¹Department of Materials Science and Engineering, University of Florida, Gainesville, Florida 312611, USA

²Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida 312611, USA

³Department of Chemical Engineering, University of Florida, Gainesville, Florida 312611, USA

^{*}Electrochemical Society Member.

^{**}Electrochemical Society Fellow.

^zE-mail: ribhusharma@ufl.edu

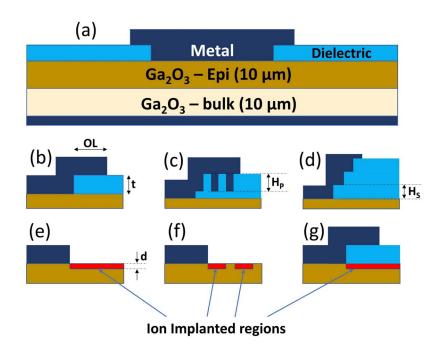


Figure 1. (a) Structure of the simulated Schottky diode based on literature. (b) Field-plated diode structure with 2 variables, i.e. Field plate overlap (OL) and dielectric thickness (t). (c) Field-plated diode pillar dielectric structure with a variable pillar height (H_P) . (d) Field-plated diode step dielectric structure with variable step height (H_S) . (e-g) Various structures simulated with Argon ion implanted resistive regions. The optimized solution between the ion implanted structures (e-g) according to the simulations would be (e) i.e. a highly resistive infinite implanted region.

extension to Tcl language for easy specification of PDEs and boundary conditions. The non-linear equations that are solved within are done so by the newton method and they are discretized in space using the finite-element method. In this work, we apply a two-dimensional model of the device structure to solve for the electric field distribution in the device. The model includes the common device equations like the Poisson's, continuity and current density equations. We solve for the electric field $|\vec{E}|$ by taking the gradient of the electrostatic potential obtained from the Poisson's equation.

In this work, the device design is optimized by studying the effect of dimensionality, structural variations and dielectric material on the reverse breakdown characteristics of vertical $\beta\text{-}Ga_2O_3$ Schottky barrier diodes. The model structure for the simulations given in Figure 1 is based on experimental study done on high current power rectifiers. 27,36 The device was fabricated using a bulk n^+ $\beta\text{-}Ga_2O_3$ (001) wafers grown by edge-define film-fed growth (EFG) and doped with Sn at 4.8×10^{18} cm $^{-3}$, with a Si doped n-type epitaxial layer grown by hydride vaper phase epitaxy (HVPE) with doping concentration of 2.8×10^{16} cm $^{-3}$. In our simulation, the effect of various epi-layer doping concentrations is also performed as seen in Figure 2 and we also observe that the bulk layer thickness does not affect the results, hence to reduce computing time we only simulate a 10 μ m thick substrate.

Figure 1 shows the field-plated structure used in the simulation, where the metal overlap (OL) and dielectric thickness (t) are varied to obtain the best dimensions for highest breakdown voltages. In addition to dimensionality, the suitability of the field plate dielectric material is also examined. The suitability depends on the relative permittivity, critical breakdown field strength and band offsets (Table I). This study

 ${\bf Table \, I. \, \, Summary \, of \, the \, dielectric \, properties \, for \, simulated \, electric \, field.}$

	β -Ga ₂ O ₃	SiO ₂	SiN_x	Al_2O_3	HfO ₂
Bandgap (eV)	4.6	8.7	3.4	6.9	5.4
ΔE_c to Ga_2O_3	-	2.87	-	2.23	1.3
ΔE_v to Ga_2O_3	-	1.23	-	0.07	-0.5
Bulk dielectric Constant, ε_b	10	3.9	7	9	25
Thin Film Dielectric constant, $\varepsilon_{\rm tf}$	-		,	841,36	$15.5^{41,42}$
Critical field Strength,	$5.2^{35,26}$	10	6.7^{40}	8.7^{36}	5.3^{43}
E _{cr} (MV/cm)					

also determines the breakdown characteristics of devices with $SiN_x,\,SiO_2,\,Al_2O_3$ or HfO_2 as the field plate dielectric material. Figure 1 also shows various field plate structures which predict improvement in breakdown voltage based on a study done on diamond Schottky diodes. 43 In this study, a pillar dielectric and graduated dielectric (step) geometry is examined for $\beta\text{-}Ga_2O_3$ Schottky diodes for different field plate dielectric materials, while varying the structural parameters as well.

Edge termination was simulated by forming a highly resistive region near the contact edges using ion implantation to spread the electric field in the device and prevent field crowding near the contact edge. Simulating the resistive region is achieved by incorporating a single mid-gap acceptor level (assumed to be gallium vacancy) with the implantation depth of 50 nm determined by TRIM simulation. The midgap state is incorporated using the incomplete ionization model we use exclusively for device simulations, given by Equation 1:

$$\frac{N_D^+}{N_{tot}} = \int \left(\frac{1}{1 + 2e^{\frac{E_F - E}{kT}}}\right) \left(\frac{1}{\nabla E \sqrt{2\pi}} e^{-\frac{(E - E_T)^2}{2\nabla E^2}}\right) dE, \quad [1]$$

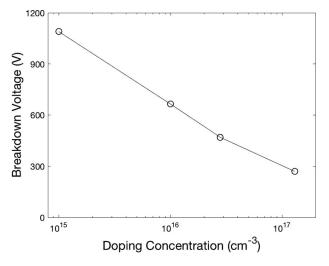


Figure 2. Breakdown voltage as a function of β -Ga₂O₃ Epi-layer doping concentration.

where N_D^+ is the ionized donor/acceptor trap concentration, N_{tot} is the total trap concentration, E_F and E_T are the electron quasi-Fermi levels and trap levels, respectively, and ∇E is the energy spread of the traps. The Full Width Half Max (FWHM) of the distribution is $2\sqrt{2ln^2}\nabla E$. The trap concentrations are obtained by using the Stopping and Range/TRansport of Ions in Matter (SRIM/TRIM) code⁴⁴ to get initial damage concentrations and using FLOOPS to simulate the Gallium vacancy diffusion during the low temperature anneal. The diffusion model for β-Ga₂O₃ is mentioned in earlier studies, ^{47,48} which uses TRIM to generate input and then produces concentration profiles after annealing is done, by specifying the temperature and time of anneal. Gallium vacancies have been identified to behave as intrinsic deep acceptors in β-Ga₂O₃ and in some cases cause compensation to n-type β-Ga₂O₃ crystals.⁴⁹ These parameters are obtained from initial work done by Gao et al.³⁵ while validation to our results is also achieved for the two dose rates i.e. 5×10^{14} cm⁻² and 1×10^{16} cm⁻². Furthermore, simulations to see the effect of using both a field plate and an ion-implanted resistive region are conducted to inform the most efficient device structure. The simulations in this work are performed for respective structures using the same mesh and the same physical parameters in order to maintain homogeneity in the results.

Results and Discussion

The breakdown voltages for the un-terminated Schottky barrier diode as a function of the epi-layer doping concentration (N_d) are revealed in Figure 2; the results match the standard trend depicting an inverse relationship between the breakdown voltage and the doping concentration which has been observed for GaN and SiC diodes. 17,22 A summary of the breakdown characteristics are shown in Table I with material parameters such as the dielectric constant, critical breakdown strength, bandgap and band offsets to β-Ga₂O₃. The breakdown voltage was calculated by the following method: FLOODS solves for the electric field being generated in the device at each element in the mesh at an applied reverse bias. The reverse bias is increased until a known critical field is achieved somewhere in the structure. The resultant 2-dimensional electric field distribution provides the location of breakdown, which is either in the epi-layer or the dielectric layer. Our results show good comparison between experimental and simulated values of un-terminated and terminated devices. 27,30,36 Breakdown is sensitive to grid spacing, so the mesh was adjusted to reliably match the baseline results. The mesh was then used for all the other results.

A simple field plate termination structure as shown in Figure 1b with the metal overlap (OL) and dielectric thickness (t) is analyzed next. Figure 3a shows the normalized breakdown voltage (V_{Nbr}) as a function of OL for the different dielectrics but with a constant dielectric thickness of 0.36 µm. The normalized breakdown voltage is obtained by normalizing to the breakdown voltage of an un-terminated β-Ga₂O₃ Schottky diode. A peak in V_{Nbr} occurs for all the dielectrics near an overlap of 1 µm, and V_{br} saturates to lower values for a field plate overlap greater than 4–5 μm. The saturation has also been observed for other studies 24,45,46 and has been seen to occur when OL approaches the depletion width at breakdown ($\sim 3-5 \mu m$ depending on V_{br} for $N_d =$ $2.8 \times 10^{16} \, \mathrm{cm}^{-3}$). This is due to the unnecessary extension of the field plate into the un-depleted semiconductor regions, assuming the lateral spread of the depletion region is comparable to the vertical spread of the depletion region. Additionally, the peak in V_{Nbr} at a field plate overlap of 1 µm is observed for structures with a dielectric thickness moderately lower than the optimal dielectric thickness (t_{opt}) . 46 t_{opt} has been found to be approximately 0.85 μ m for the β -Ga₂O₃ SBD at the specific conditions. From the data in Figure 3a and for a dielectric thickness of 0.36 µm, the rise and fall of the breakdown voltage is mainly due to the respective reduction and increase of the electric field crowding at the field plate edge in the Gallium oxide.

The simulations also suggest that in the devices with a SiO_2 or SiN_x dielectric layer, breakdown occurs in the dielectric; whereas in the devices with a Al_2O_3 or HfO_2 dielectric layer, breakdown occurs in the β -Ga $_2O_3$ epi-layer. This can be explained by the high dielec-

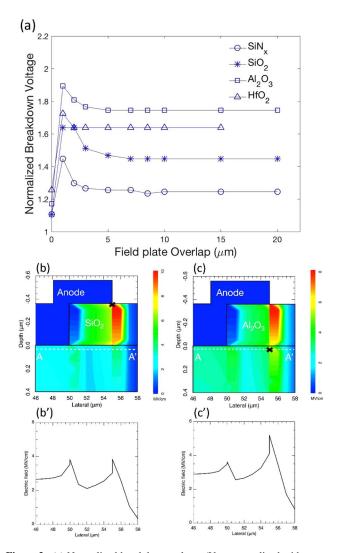


Figure 3. (a) Normalized breakdown voltage (V_{Nbr} normalized with respect to V_{br} of an unterminated SBD) as a function of field plate overlap (OL) for the four dielectrics. (b) Electric field distribution in diodes with SiO_2 as the dielectric, and (b') shows the electric field values along the A-A' line drawn in (b). (c) Electric field distribution in diodes with Al_2O_3 as the dielectric, and (c') shows electric field values along line A-A' drawn in (c). (b') and (c') show the comparison of electric field values in Ga_2O_3 epi-layer (near the interface), device is breaking down in epi-layer with Al_2O_3 as dielectric whereas the device is breaking down in the SiO_2 layer with SiO_2 as the dielectric (breakdown location marked by an "x").

tric constant (Table I) for both Al_2O_3 and HfO_2 compared to SiO_2 and SiN_x , which means the β - Ga_2O_3 reaches its critical field before Al_2O_3 and HfO_2 can reach their critical fields, whereas SiO_2 and SiN_x reach their critical field before β - Ga_2O_3 as the reverse bias voltage is increased. Breakdown locations for SiO_2 and Al_2O_3 field plated β - Ga_2O_3 Schottky diode structures ($OL=5~\mu m$) are shown in Figures 3b and 3c.

Similarly, Figure 4a shows the normalized breakdown voltage as a function of the dielectric thickness t, for the four different FP dielectrics considered in this study while the OL is kept constant at $10\,\mu\text{m}$. Intuitively, as the FP dielectric thickness is increased the breakdown voltage should also increase, as the electric field magnitude is inversely proportional to the dielectric thickness. However, as stated earlier the effects of the dielectric constant causes the early breakdown of larger thicknesses in low ε dielectrics. This effect can be seen in Figure 4a as we see discontinuity in the breakdown voltage as t is increased for SiO_2 and HfO_2 . This discontinuity is explained by the breakdown location shifting from the dielectric to the β - Ga_2O_3

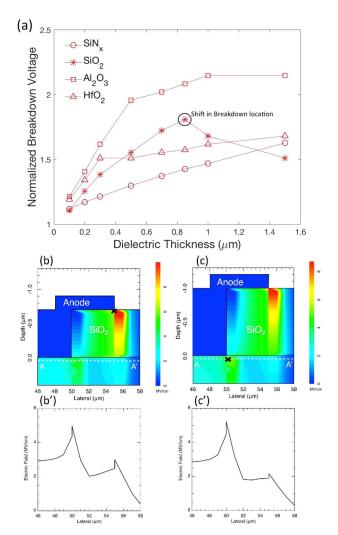


Figure 4. (a) Normalized breakdown voltage (V_{Nbr} normalized with respect to V_{br} of an unterminated SBD) as a function of field plate dielectric thickness (t) for the four dielectrics. Electric field distribution for SiO₂ dielectric field plate for $t=0.7~\mu m$ (b) and $t=1.0~\mu m$ (c). (b') Electric field values along A-A' drawn in (b). (c') Electric field values along A-A' drawn in (c). (b') and (c') show the comparison of electric field values in Ga_2O_3 epi-layer (near the interface), device breakdown location shifts from the SiO₂ to the Ga_2O_3 epi-layer as t exceeds $0.85~\mu m$ (breakdown location marked by an "x").

epi-layer or vice versa. Figures 4b and 4c help visualize this shift in the breakdown location for a device with SiO_2 as the FP dielectric. We observed a shift in breakdown location from the dielectric layer to the β -Ga $_2$ O $_3$ epi-layer at a thickness of 0.85 μ m, while the figure compares two simulation results for a t of 0.7 and 1.0 μ m.

Å similar study was performed by Arbess et al. 43 on a high-voltage diamond Schottky diode, where different FP structures like a pillar structure and a graduated dielectric form seen in Figure 1 are examined. This study along with previous studies on such diodes have shown that the maximum electric field is located just below the metal corners; and to mitigate this effect, corners are added to distribute the peaks. As shown in Figures 1c and 1d, this study focuses on one parameter for each structure i.e. the pillar height and the step height of the dielectric. As seen in Figure 5, for the graduated (step) dielectric form a $V_{\rm Nbr}$ of about 3 is observed for a step height of 1 μ m for a Al_2O_3 dielectric. These results indicate that by using a graduated dielectric (or a tapered dielectric) FP a higher breakdown voltage can be achieved compared to a normal dielectric FP of the same total thickness.

In order to study edge termination via ion implantation, the Schottky barrier diode is simulated with Ar ion implantation to form a highly resistive region at the periphery of the anode contact. GaO et al.³⁴ per-

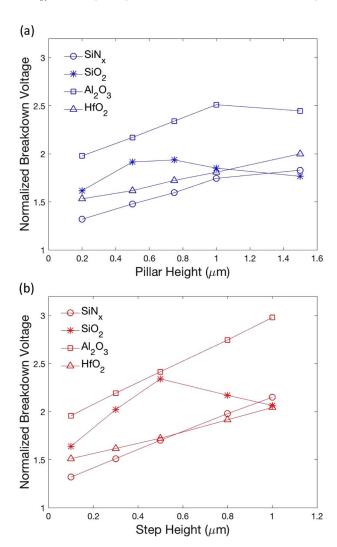


Figure 5. (a) Normalized breakdown voltage (normalized with respect to V_{br} of an unterminated SBD) as a function of pillar height (H_P) for the four dielectrics, with a V_{Nbr} of 2.5 achieved for device with Al_2O_3 as the dielectric $(H_P=1.0\,\mu m)$. (b) Normalized breakdown voltage as a function of step height (H_S) for the four dielectrics, with a V_{Nbr} of over 3 achieved for device with Al_2O_3 as the dielectric $(H_S=1.0\,\mu m)$.

formed the study for two different implant doses, while in this work the breakdown voltage is extracted as a function of the trap concentration after implantation and subsequent annealing. Figure 6 shows a plot of normalized breakdown voltage (V_{Nbr}) vs the trap concentration (N_{MG}) of the midgap acceptor trap in the resistive region with a depth of 50 nm, at different epi-layer doping levels for a β -Ga₂O₃ Schottky barrier diode. A V_{Nbr} of over five is achieved for a diode with epi-layer doping as 2.8×10^{16} cm⁻³, while a V_{Nbr} of approximately two is achieved for a diode with epi-layer doping as 1.3×10^{17} cm⁻³. The curves level out for trap concentrations near and over 10^{19} cm⁻³ which is because the ideal plane parallel breakdown voltage determined for this device^{21,34} is reached at $\sim 10^{19}$ cm⁻³ N_{MG} values. As observed in previous studies, the breakdown location shifts from the contact edge, to the edge of the resistive region 50 nm below the contact edge.

Furthermore, we also simulated the structure in Figure 1f where multiple finite-implanted regions are formed and we achieve a $V_{\rm Nbr}$ < 2, hence suggesting devices with multiple implanted regions or finite implanted regions do not perform as well as devices with infinite implanted regions as seen in Figure 1e. This can be explained by the limited electric field spreading (or increased field crowding at corners) when multiple implanted regions are produced, compared to an infinite implanted region where a superior field spreading (or lower

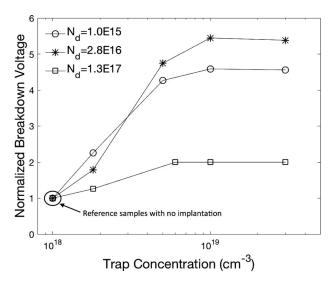


Figure 6. Normalized breakdown voltage as a function of midgap acceptor trap (gallium vacancy) concentration (N_{MG}) for different epi-layer doping concentrations. V_{lr} has been normalized with respect to the breakdown voltage of non-terminated diodes, and the values for V_{br} for N_d of 1×10^{15} , 2.8×10^{16} and 1.3×10^{17} cm $^{-3}$ are 1090, 470 and 270 V respectively for unterminated diodes. The ideal plane parallel breakdown voltage is reached for the device with N_{MG} greater than 10^{19} cm $^{-3}$.

field crowding) is expected. For devices with both a field-plate and an ion implanted resistive region as seen in Figure 1f, the spreading of the electric field within the Ga_2O_3 epi-layer prevents any potential from being developed in the dielectric hence making the field plate ineffective. Finally, the breakdown voltage is simulated as a function of the depth (d) of the resistive region as seen in Figure 7a. Maximum value for V_{br} is achieved for a depth of 75nm, and we see a gradual drop in V_{br} as the depth of this region is increased, which could be attributed to increased resistance as the depth of the resistive region is increased. Further simulations reveal that due to the resistive area we observe bending of the electrostatic potential lines laterally across the device. The bending is observed just below the resistive area edge under the contact edge. As d is increased the electric field crowding near the resistive area edge increases, which results in a decline in V_{br} .

We also simulated the diffusion of the gallium vacancies after the argon implantation and developed a model to accurately predict the concentration of midgap acceptor traps (N_{MG}) . The concentrations achieved replicate the breakdown characteristics of diodes studied by Gao et al. 34 where the $5\times10^{14}~\rm cm^{-2}$ implant dose corresponds to a N_{MG} value of $1.80\times10^{18}~\rm cm^{-3}$ and a $1\times10^{16}~\rm cm^{-2}$ implant dose corresponds to an N_{MG} value of $3.0\times10^{19}~\rm cm^{-3}$. The simulated concentration profiles of the midgap acceptor traps (gallium vacancies) are seen in Figure 7b for the two dose rates. This model would help in obtaining the gallium vacancy concentration after argon implantation at different implantation energies by using TRIM to simulate the initial damage concentrations, and then using the FLOOPS model to simulate the damage annealing and vacancy diffusion.

Conclusions

Edge termination for vertical $\beta\text{-}Ga_2O_3$ Schottky diodes was analyzed by simulating the electric field distribution in the diodes as the reverse bias is increased. The breakdown location of these Schottky diodes was located, and the field crowding near the contact edge was mitigated by utilizing edge termination techniques like field plates and highly-resistive implanted regions. Al $_2O_3$ is established as the superior field plate dielectric compared to $SiO_2,\,SiN_x,$ and HfO_2 by demonstrating V_{Nbr} of over 2 for standard field-plated diodes, while a V_{Nbr} of over 3 is achieved for the graduated form dielectric field-plated diode. Edge termination via argon implantation near the contact edges

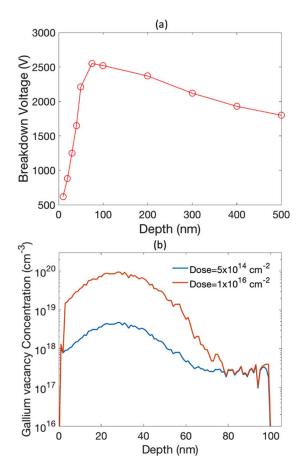


Figure 7. (a) Breakdown voltage as a function of the depth of the resistive (Argon ion implanted) region, for device with $N_d = 2.8 \times 10^{16} \text{ cm}^{-3}$. (b) Concentration profile of gallium vacancies (midgap acceptor trap N_{MG}) after the sample was implanted with Argon ions at 50 keV (TRIM) and annealed for 60 seconds at 400°C under N_2 ambient (FLOOPS).

has resulted in even higher breakdown voltages for these diodes with a $V_{\rm Nbr}$ of $\sim\!\!5$ reported in this work. Furthermore, this technique is investigated in terms of the formation of deep acceptor states (gallium vacancies), diffusion of the gallium vacancies, depth of the resistive region, implantation energy and annealing parameters to develop a model to simulate this edge termination technique.

Acknowledgments

The project was sponsored by the Department of the Defense, Defense Threat Reduction Agency, HDTRA1-17-1-011, monitored by Jacob Calkins and also by NSF DMR 1856662 (Tania Paskova).

ORCID

Ribhu Sharma https://orcid.org/0000-0001-5754-7873 S. J. Pearton https://orcid.org/0000-0001-6498-1256

References

- W. Lee, S. Li, D. Han, B. Sarlioglu, T. A. Minav, and M. Pietola, *IEEE Transactions on Transportation Electrification*, 4, 684 (2018).
- on Transportation Electrification, 4, 684 (2018). 2. A. Q. Huang, Proceedings of the IEEE, 105, 2019 (2017).
- V. Veliadis, R. Kaplar, J. Zhang, M. Bakowski, S. Khalil, and P. Moens, *IEEE Power Electronics Magazine*, 5, 45 (2018).
- S. J. Pearton, J. Yang, P. H. Carey, F. Ren, K. Jihyun, M. J. Tadjer, and M. A. Mastro, *Applied Physics Reviews*, 5, 11301 (2018).
- E. Hoene, G. Deboy, C. R. Sullivan, and G. Hurley, IEEE Power Electronics Magazine, 5, 28 (2018).

- A. Pérez-Tomás, E. Chikoidze, M. R. Jennings, S. A. O. Russell, F. H. Teherani, P. Bove, E. V. Sandana, and D. J. Rogers, *Oxide-based Materials and Devices IX*, *Proc. SPIE* 10533, (2018).
- F. Roccaforte, P. Fiorenza, G. Greco, R. Lo Nigro, F. Giannazzo, F. Iucolano, and M. Saggio, *Microelectronic Engineering*, 187–188, 66 (2018).
- R. J. Kaplar, A. A. Allerman, A. M. Armstrong, M. H. Crawford, J. R. Dickerson, A. J. Fischer, A. G. Baca, and E. A. Douglas, *ECS Journal of Solid State Science and Technology*, 6, Q3061 (2017).
- "RAVPower Premium Portable Charger, External Battery, USB wall charger, travel charger, car charger, wireless charger, solar charger, cell phone batteries,", Ravpower.com, 2018. Online]. Available: https://www.ravpower.com/promo/ power-delivery.
- Z. Galazka, R. Uecker, D. Klimm, K. Irmscher, M. Naumann, M. Pietsch, A. Kwasniewski, R. Bertram, S. Ganschow, and M. Bickermann, *ECS Journal of Solid State Science and Technology*, 6, Q3007 (2017).
- S. Ghose, S. Rahman, L. Hong, J. S. Rojas-Ramirez, H. Jin, K. Park, R. Klie, and R. Droopad, *Journal of Applied Physics*, 122, 95302 (2017).
- M.-Y. Tsai, O. Bierwagen, M. E. White, and J. S. Speck, *Journal of Vacuum Science & Technology A*, 28, 354 (2010).
- Y. Yao, S. Okur, L. A. M. Lyle, G. S. Tompa, T. Salagaj, N. Sbrockey, R. F. Davis, and L. M. Porter. *Materials Research Letters*, 6, 268 (2018).
- M. Baldini, Z. Galazka, and G. Wagner, Materials Science in Semiconductor Processing, 78, 132 (2018).
- A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui, and S. Yamakoshi, Japanese Journal of Applied Physics, 55, 1202A2 (2016).
- Y. Chen, X. Xia, H. Liang, Q. Abbas, Y. Liu, and G. Du, Crystal Growth & Design, 18, 1147 (2018).
- Y. Lei, H. Shi, H. Lu, D. Chen, R. Zhang, and Y. Zheng, *Journal of Semiconductors*, 34, 54007 (2013).
- J. R. Laroche, F. Ren, K. W. Baik, S. J. Pearton, B. S. Shelton, and B. Peres, *Journal of Electronic Materials*, 34, 370 (2005).
- K. H. Baik, Y. Irokawa, F. Ren, S. J. Pearton, S. S. Park, and S. K. Lee, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 20, 2169 (2002).
- 20. A. M. Ozbek and B. J. Baliga, IEEE Electron Device Letters, 32, 1361 (2011).
- 21. A. M. Ozbek and B. J. Baliga, *IEEE Electron Device Letters*, 32, 300 (2011).
- M. C. Tarplee, V. P. Madangarli, Quinchun Zhang, and T. S. Sudarshan, *IEEE Transactions on Electron Devices*, 48, 2659 (2001).
- 23. A. Itoh, T. Kimoto, and H. Matsunami, IEEE Electron Device Letters, 17, 139 (1996).
- V. Soler, M. Berthou, A. Mihaila, J. Monserrat, P. Godignon, J. Rebollo, and J. Millán, Semiconductor Science and Technology, 32, 35007 (2017).
- S. Nigam, J. Kim, B. Luo, F. Ren, G. Y. Chung, S. J. Pearton, J. R. Williams, K. Shenai, and P. Neudeck, *Solid-State Electronics*, 47, 57 (2003).

- K. Konishi, K. Goto, H. Murakami, Y. Kumgai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, Appl. Phys. Lett., 110, 103506 (2017).
- J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, ECS Journal of Solid State Science and Technology, 7, Q92 (2018).
- J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, AIP Advances, 8, 55026 (2018).
- J. Yang, F. Ren, S. J. Pearton, and A. Kuramata, *IEEE Transactions on Electron Devices*, 1 (2018).
- Z. Hu, H. Zhou, Q. Feng, J. Zhang, C. Zhang, K. Dang, Y. Cai, Z. Feng, Y. Gao, X. Kang, and Y. Hao, *IEEE Electron Device Letters*, 39, 1564 (2018).
- C. Lin, Y. Yuda, M. H. Wong, M. Sato, N. Takekawa, K. Konishi, T. Watahiki, M. Yamamuka, H. Murakami, Y. Kumagai, and M. Higashiwaki, in 2019 Compound Semiconductor Week (CSW), p. 1 (2019).
- 32. J. L. Lyons, Semiconductor Science and Technology, 33, 05LT02 (2018).
- L. Dong, R. Jia, C. Li, B. Xin, and Y. Zhang, Journal of Alloys and Compounds, 712, 379 (2017).
- 34. J.-H. Choi, C.-H. Cho, and H.-Y. Cha, *Results in Physics*, 9, 1170 (2018).
- Y. Gao, A. Li, Q. Feng, Z. Hu, Z. Feng, K. Zhang, X. Lu, C. Zhang, H. Zhou, W. Mu, Z. Jia, J. Zhang, and Y. Hao, Nanoscale Research Letters, 14, 8 (2019).
- P. H. Carey, J. Yang, F. Ren, R. Sharma, M. E. Law, and S. J. Pearton, ECS Journal of Solid State Science and Technology.
- 37. M. E. Law and S. M. Cea, Computational Materials Science, 12, 289 (1998).
- 38. K. Hirose, H. Kitahara, and T. Hattori, *Phys. Rev. B*, 67, 195313 (2003).
- 39. S. M. Sze, Journal of Applied Physics, 38, 2951 (1967).
- A. E. Kaloyeros, F. A. Jové, J. Goff, and B. Arkles, ECS Journal of Solid State Science and Technology, 6, P691 (2017).
- M. J. Biercuk, D. J. Monsma, C. M. Marcus, J. S. Becker, and R. G. Gordon, *Appl. Phys. Lett.*, 83, 2405 (2003).
- A. Taube, S. Gieraltowska, T. Gutt, T. Malachowski, I. Pasternak, T. Wojciechowski, W. Rzodkiewicz, M. Sawicki, and A. Piotrowska, *Acta Physica Polonica*, A., 119, 696 (2011).
- H. Arbess, K. Isoird, S. Hamady, M. Zerarka, and D. Planson, *IEEE Transactions on Electron Devices*, 62, 2945 (2015).
- 44. Stopping and Range of ions in Matter (SRIM), available at http://www.srim.org/#SRIM.
- 45. S.-K. Chung and S.-Y. Han, Microelectronics Journal, 33, 399 (2002).
- 46. C. B. Goud and K. N. Bhat, IEEE Transactions on Electron Devices, 38, 1497 (1991).
- R. Sharma, E. Patrick, M. E. Law, S. Ahn, F. Ren, S. J. Pearton, and A. Kuramata, *ECS Journal of Solid State Science and Technology*, 6, P794 (2017).
- R. Sharma, M. E. Law, C. Faker, F. Ren, A. Kuramata, and S. J. Pearton, *AIP Advances*, 9, 85111 (2019).
- B. E. Kananen, L. E. Halliburton, K. T. Stevens, G. K. Foundos, and N. C. Giles, *Appl. Phys. Lett.*, 110, 202104 (2017).