



## Trapping Phenomena in InAlN/GaN High Electron Mobility Transistors

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Electron trapping-detrapping phenomena were studied for InAlN/GaN high electron mobility transistors (HEMTs) by drain current-drain voltage static and pulsed current voltage (I-V) characteristics, gate current I-Vs, transfer characteristic measurements, current deep level transient spectroscopy (CDLTS) with gate voltage pulsing, and by drain current transient measurements following both drain and gate voltage steps. The electron trapping processes are temperature activated with activation energies of 1.1 eV for drain voltage steps and 1 eV and 0.75 eV for gate voltage steps. Detrapping processes show activation energies 0.9 eV and (0.7–0.75) eV. Drain current transients are accurately described by the sum of two stretched exponents. The amplitudes of CDLTS peaks corresponding to electron trapping and electron detrapping processes show a logarithmic dependence on the width of the injection pulse, indicating that the traps are related to dislocations.

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InAlN/GaN heterojunctions provide an alternative to AlGaIn/GaN for use in high electron mobility transistors (HEMTs) with high power capability.<sup>1–8</sup> The advantages of InAlN/GaN heterojunctions compared to the AlGaIn/GaN system include a very high spontaneous electrical polarization resulting in two-dimensional electron gas (2DEG) density of about  $2.7 \times 10^{13} \text{ cm}^{-2}$ , about twice as high as for AlGaIn/GaN.<sup>1–8</sup> The InAlN barrier layer can be made closely lattice matched to GaN for In mole fraction of ~18%.<sup>1–8</sup> The resulting decrease of strain and the absence of piezoelectric polarization should be beneficial for HEMTs' reliability and can potentially reduce current collapse phenomena in InAlN/GaN HEMTs.<sup>8,9</sup> These advantages lead to superior device performance of InAlN/GaN HEMTs in some aspects to AlGaIn/GaN HEMTs.<sup>10</sup> However, the growth technology for InAlN with high crystalline quality and low impurity contamination is demanding because the films have to be deposited at relatively low temperatures of around 800°C to prevent In evaporation from the growing surface.<sup>10</sup> This usually results in higher dislocation densities and higher contamination by impurities, particularly oxygen.<sup>11</sup> It is not unusual to observe residual donor concentrations in InAlN on the order of  $10^{18} \text{ cm}^{-3}$ .<sup>11</sup> Dislocation cores in InAlN have been shown to be decorated by In giving rise to excessive leakage.<sup>12,13</sup> All this commonly results in the gate leakage currents of HEMTs with InAlN barriers being much higher than for AlGaIn barriers.<sup>14</sup>

Detailed studies of the gate current in InAlN HEMTs point to the predominance of the Poole-Frenkel emission mechanism.<sup>14</sup> Deep level studies on InAlN films and InAlN/GaN HEMT structures often reveal the presence of a high concentration of deep electron traps with energy levels between 0.08 and 1 eV.<sup>14–17</sup> The traps with energy levels near  $E_c - 0.08$  and  $E_c - 0.26$  eV show clear signs of metastability, similar to the behavior of DX-defects.<sup>11</sup> Deep traps in the InAlN barrier causing changes in the threshold voltage of HEMTs.<sup>16,17</sup> InAlN/GaN heterojunctions have been shown to be more susceptible to changes in 2DEG concentration and mobility upon electron and neutron irradiation compared to their AlGaIn/GaN counterparts.<sup>18,19</sup>

Recent advances in material quality of InAlN barrier layers and InAlN/GaN heterojunctions have led to decreases in gate leakage current and performance of HEMTs,<sup>20</sup> but the current flow mechanisms and trapping effects in such improved HEMT structures are still not fully understood. In this paper, we present results obtained by pulsed current-voltage I-V measurements, current deep level transient spectroscopy (CDLTS), and by detailed analysis of the drain current transients performed over a range of temperatures. The CDLTS approach provides a rapid assessment tool to roughly characterize the

state of deep traps in the improved InAlN/GaN HEMTs studied in this paper. Two prominent traps with levels near  $E_c - (0.7 - 0.75)$  eV and  $E_c - (1 - 1.1)$  eV were dominant and the logarithmic dependence of respective CDLTS peaks on the pulse length indicates that the said traps could be related to dislocations. Detailed current transients analysis provides more accurate characterization of the drain current decay waveforms. It is shown that the transients are not pure exponents, as assumed in CDLTS, but can be represented by a sum of two stretched exponents. This approach provides a more accurate determination of the activation energies and relative impact of the two contributions in detrapping phenomena in InAlN/GaN HEMTs. We also provide for the first time detailed analysis of the trapping phenomena in our advanced InAlN/GaN HEMTs.

### Experimental

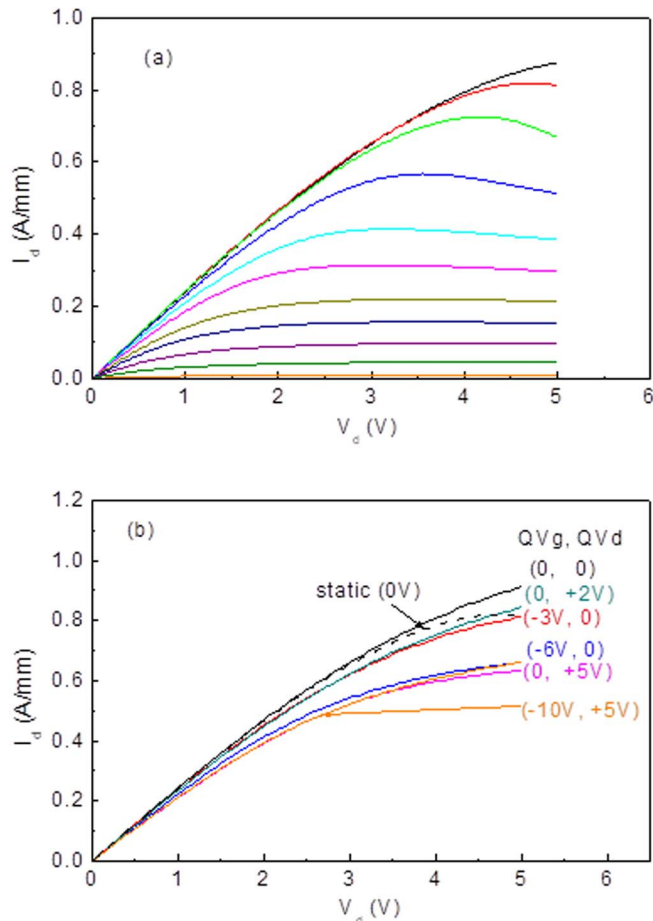
InAlN HEMT structures were grown by metallorganic chemical vapor deposition on sapphire. The structure consisted of 1.9 μm semi-insulating GaN buffer, 55 nm GaN channel layer lightly Si doped, and 28-nm-thick InAlN barrier with In mole fraction of 17%. The distance between source and drain was 10 μm, the gate length was 1 μm, the gate width was 200 μm. Ohmic contacts for the source and drain were fabricated by lift-off of E-beam deposition of Ti/Al/Ni/Au. Schottky diode gates were fabricated by lift-off of the E-beam deposited Ni/Au layers.

Static and pulsed drain-source and transfer characteristics were measured using B2902A (Keysight Technologies, USA) current/voltage/source/meter for temperatures in the range 80–400 K using an Oxford Instruments (UK) gas-flow cryostat, and, for temperatures from above room temperature up to 500 K, in a custom-built hot plate system.

The impact of deep traps on I-V characteristics was assessed by comparing static I-V characteristics with pulsed I-V characteristics, measured with different quiescent points.<sup>21</sup> Characteristics of deep traps involved in current collapse were obtained from current deep level transient spectroscopy (CDLTS) measurements upon pulsing of the gate voltage, drain voltage or both.<sup>22–24</sup> CDLTS measurements provide an evaluation tool for rapid characterization of trapping in GaN HEMTs, but are subject to uncertainties regarding the impact of the pulse length and the actual waveform of current transients.<sup>23–25</sup> Because of this, we also performed analysis of current transients occurring upon application of gate voltage and drain voltage steps over a wide range of temperatures. The exact waveform of the transients was obtained by fitting of gate current or drain current transients  $I = I(t)$  and transient current derivatives by the logarithm of time

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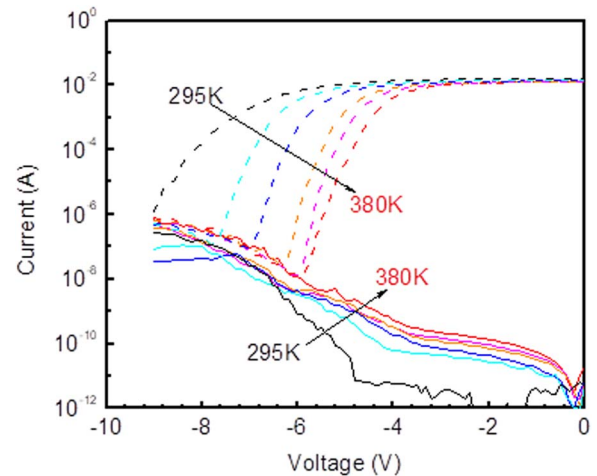


**Figure 1.** (a) Static normalized drain current versus drain voltage I-V characteristics measured for different gate voltages from +1 V to -10 V (gate voltage step of 1 V); (b) pulsed drain I-V characteristics measured for gate voltage 0 V and different quiescent points QVg and QVd of (0 V, 0 V, black line), (0, +2 V, olive line), (-3 V, 0 V, red line), (-6 V, 0 V, blue line), (0, +5 V, magenta line), (-10 V, +5 V, orange line), also shown is the static I-V for  $V_g = 0$  V.

$I' = dI(t)/d(\ln(t))$  using several stretched exponents of the form  $I = A(\exp[-(t/\tau)^\beta])^{23-25}$  and finding the set of amplitudes  $A$ , relaxation times  $\tau$ , and broadening factors  $\beta$  producing the best match to experimental  $I(t)$  and  $dI(t)/d(\ln(t))$  curves for the number of stretched exponents chosen based on the number of peaks observed in current derivatives. For the transistors studied here, no more than two exponents were necessary to obtain good fitting. Temperature-dependent measurements then allowed the calculation of the activation energies of the processes involved in capture and emission from the temperature dependencies of relaxation times  $\tau$ . The data analysis procedure is described in detail elsewhere.<sup>23,25</sup>

## Results

**Drain current static and pulsed I-V characteristics.**—Fig. 1a presents the drain current  $I_d$  dependence on source-drain voltage  $V_d$  for gate voltages ranging from +1 V to -10 V. The normalized saturation current at 0 V gate voltage in the figure is 0.8 A/mm. At low gate voltages, some negative differential resistance owing to the device heating is observed. Fig. 1b compares static (dashed curve) and pulsed (solid curves) drain I-V characteristics measured at 0 V gate voltage with double pulses with quiescent points in the gate voltage  $QV_g$  and in the drain voltage  $QV_d$  shown near each curve. The pulse width for both measurement pulses was 0.2 ms and the period was 100 ms. Fig. 1b shows that, for both  $QV_g$  and  $QV_d$  equal to zero, the pulse



**Figure 2.** Drain current dependence on gate voltage for drain voltage  $V_d = 0.5$  V (dashed curves) measured at several temperatures between 295 K and 380 K; also shown the dependence of gate current on gate voltage at  $V_d = 0$  V (solid lines) for the same temperatures; the data shown for  $T = 295$  K (black lines), 325 K (cyan lines), 340 K (blue lines), 360 K (orange lines), 370 K (magenta lines), and 380 K (red lines).

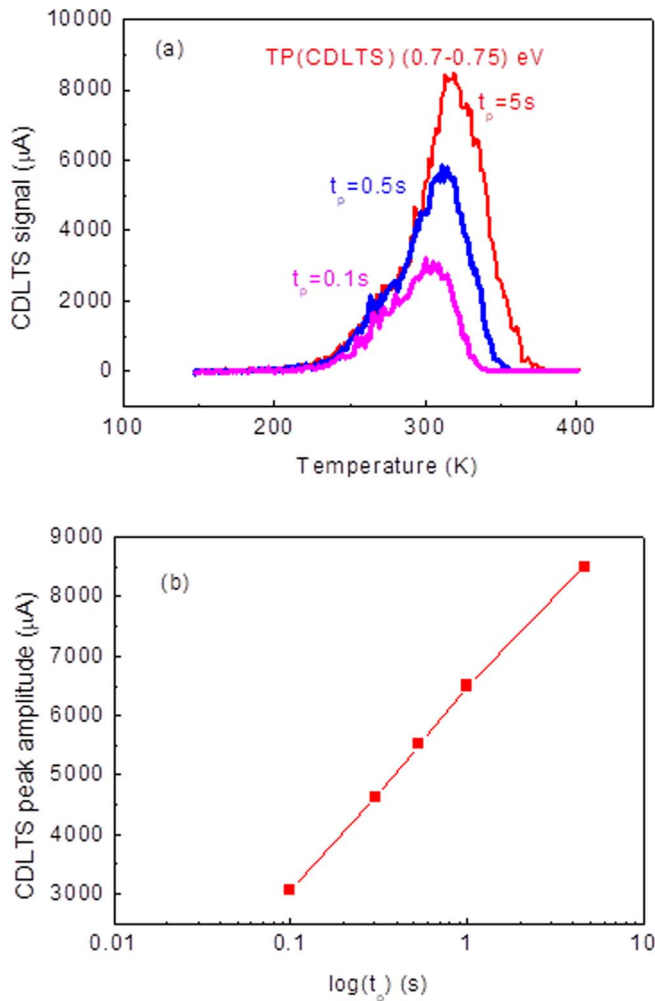
I-V curve at high drain voltages is substantially higher than the static characteristic because of reduced heating effects. The application of high quiescent gate voltages and/or drain voltages leads to substantial current decrease at high drain voltages and to an increase of on-state resistance  $R_{ON}$  in the linear I-V region. The changes in these values are  $\sim 25\%$  at high gate voltage or drain voltage (or both voltages) pulses.

## Transfer I-V characteristics and gate current I-V characteristics.

—Fig. 2 shows the evolution of the drain current at drain voltage of 0.5 V as a function of gate voltage  $V_g$  as temperature was slowly increased from room temperature to 400 K. The results are compared to the dependence of the gate current  $I_g$  on gate voltage. The threshold voltage of the InAlN/GaN HEMT changes with temperature and the drain current in the OFF state is mainly determined by the gate current. The temperature dependence of the gate current shows an activation energy of 0.35 eV at low gate voltages and 0.55 eV at high gate voltages. The data published in the literature strongly vary in terms of the effective Schottky barrier height for Ni/InAlN, from about 0.5 eV,<sup>10</sup> to (0.7–1.5) eV.<sup>26,27</sup> Detailed analysis suggests that the spread could be the result of the Schottky barrier height fluctuations caused by the local InAlN composition fluctuations.<sup>27</sup> The resulting reverse current density could then be reasonably approximated by combined action of Fowler-Nordheim tunneling and Poole-Frenkel current flow via electron tunneling into deep traps with levels approximately aligned with the Fermi level in Schottky barrier metal and subsequent thermal excitation into the dislocation states band centered close to 0.5 eV from the local conduction band edge. The lower reverse current of the studied Schottky diodes compared to previous reports are likely due to lower In composition fluctuations and higher effective Schottky barrier. The direct tunneling into the buffer is perhaps not an issue in our case (consider the relatively high activation energy of the gate current at high reverse voltages).

**CDLTS spectra.**—Charge trapping in our InAlN/GaN HEMT upon gate and drain pulsing was studied by CDLTS measurements in several regimes.

**Regime 1.**—The gate voltage  $V_g$  was pulsed from below  $V_{th}$  (-9 V) to 0 V, the drain voltage  $V_d$  was 0.5 V (linear region in drain I-Vs), the pulse length was varied from 0.1 s to 5 s, the drain current  $I_d(t)$  transient was monitored and the temperature dependence of



**Figure 3.** (a) CDLTS spectra of InAlN/GaN HEMT measured at  $V_g = -9$  V,  $V_d = 0.5$  V,  $V_g$  pulse from  $-9$  V to 0 V, the three spectra are shown for pulse durations  $t_p = 0.1$  s (red line),  $0.5$  s (blue line),  $5$  s (magenta line) (see labels near the spectra), time windows  $t_1/t_2 = 30$  ms /600 ms; (b) the dependence of the CDLTS peak amplitude on the logarithm of pulse duration  $t_p$ .

$\Delta I_d = I_d(t_1) - I_d(t_2)$  was determined as a function of the chosen time windows  $t_1$  and  $t_2$ . Fig. 3a shows such spectra for time windows  $t_1 = 30$  ms,  $t_2 = 600$  ms and three pulse lengths  $t_p = 0.1$  s,  $0.5$  s,  $5$  s. A positive CDLTS peak corresponding to the drain current decreasing with time after the end of the pulse can be clearly seen. Such drain current transient sign indicates the increase with time of the negative charge trapped on defects and can be attributed either to the emission of holes from hole traps<sup>25</sup> or to electron capture by electron traps after the end of the pulse caused by the re-application of reverse gate voltage pulse<sup>23–25</sup> (in the latter case during the pulse the traps emit part of the captured electrons that are re-trapped after the end of the pulse). If we are dealing with hole emission, the activation energy of the process is the depth of the hole traps, while the exponential pre-factor yields the capture cross section for holes. If the drain current decrease is caused by electrons being trapped at high reverse gate voltage after the pulse, the activation energy of the process characterizes the effective barrier for capture that has to be overcome and the meaning of the pre-factor needs an understanding of the temperature activated capture mechanism. For example, Joh and Alamo<sup>27</sup> observed such a temperature activated capture process and attributed it to thermally assisted tunneling into the AlGaN barrier in AlGaN/GaN HEMTs, with subsequent capture of electrons by deep traps in the barrier. Previous work<sup>23,24</sup> proposed an alternative mechanism in which the observed phenomenon is due to tunneling into dislocation-related states and

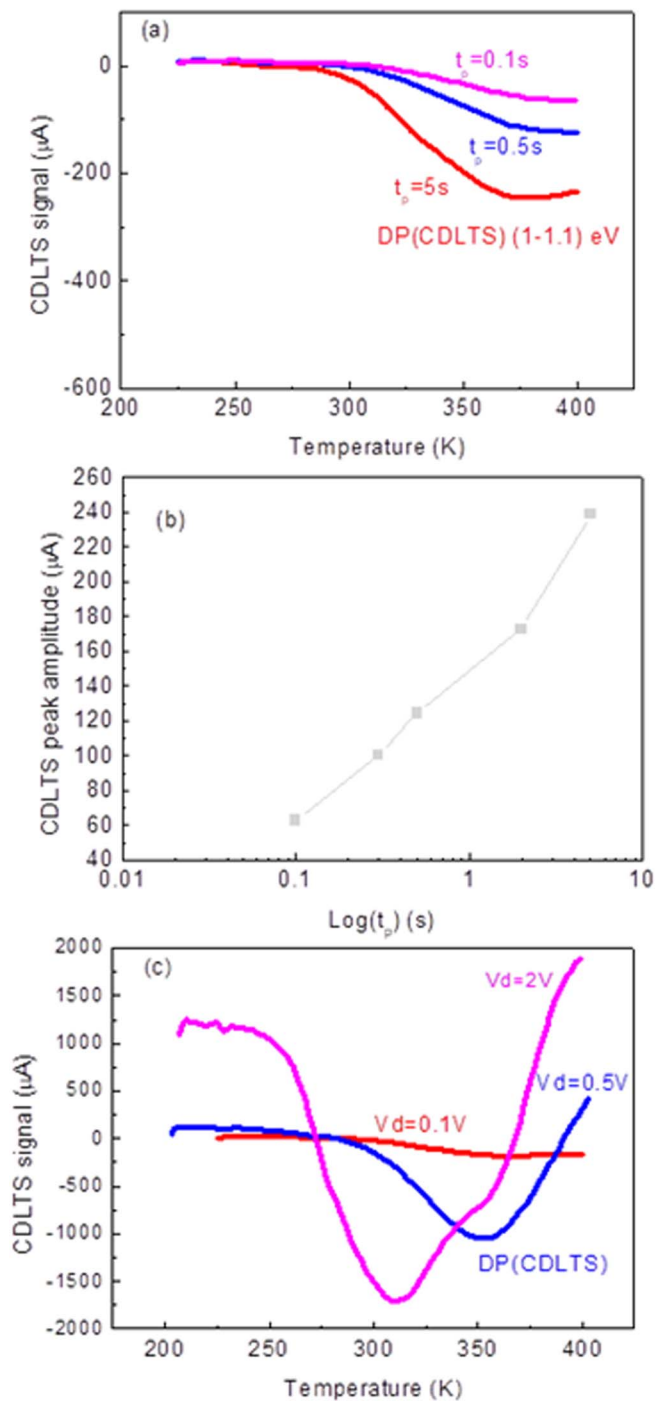
movement of the trapped charge toward the AlGaN/GaN interface by excitation of trapped electrons into the percolation band of dislocations and repeated trapping/detrapping by the dislocation states, so that the charge front is a multistage process of detrapping, drift and re-trapping. The decrease of the drain current upon application of high gate voltage is due to the negative charge front approaching the AlGaN/GaN interface. In principle, changing the direction of the voltage step can change the direction of the drain current change and give rise to CDLTS peak of opposite sign and similar activation energy (but not necessarily the same pre-exponential factor or the apparent charge capture cross section in traditional CDLTS parlance).<sup>25</sup> For our InAlN/GaN HEMTs, the activation energy of the trapping process TP(CDLTS) was (0.7–0.75) eV. The amplitude of the CDLTS peak logarithmically increased with the pulse length  $t_p$  as illustrated by Fig. 3b.

**Regime 2.**—In this regime, we used the steady-state  $V_g = 0$  V or  $-2$  V (transistor ON or semi-ON),  $V_g$  was pulsed down to below the threshold voltage, to  $V_g = -9$  V (OFF-state), the drain voltage was 0.1 V, 0.5 V or 2 V. The OFF-state  $V_g$  voltage pulse length was varied from 0.1 s to 5 s as in Regime 1. We monitored the drain current recovery after the OFF state. The results for steady-state  $V_g = 0$  V or  $-2$  V were qualitatively very similar so we show only the data for  $V_g = 0$  V. The spectra measured with  $V_d = 0.1$  V and pulse lengths of 0.1 s, 0.5 s, and 5 s are shown in Fig. 4a. The main feature of the spectra was the negative CDLTS peak near 380 K corresponding to the drain current increase with time after the  $V_g$  OFF pulse. This drain current increase with time caused by negative charge detrapping process DP (CDLTS) had the activation energy of (1–1.1) eV. The magnitude of the peak logarithmically increased with the pulse length as shown in Fig. 4b. Increasing the drain voltage led to the appearance of positive features in CDLTS related to the drain current transient becoming a mixture of rising (detrapping) and falling (trapping)  $I_d(t)$  regions. These positive features corresponding to the charge trapping (drain current decreasing with time after the pulse) produced serious distortion of the main negative peak DP (CDLTS) amplitude near 380 K and the appearance of a negative quasi-peak near 300 K for the high drain voltages (Fig. 4c). These distortions were the result of charge trapping by the states in the gate-drain access region or the buffer when a high drain current was flowing through the transistor in the ON or semi-ON state. Accurate measurements of the waveforms and the relaxation times as a result of changing biasing conditions and temperature after a step-wise change of gate or drain biases shed additional light on the nature of the processes involved.

**Current relaxations after step-wise voltage changes.**—Two major regimes of drain current transient measurements following the application of a step in the drain voltage were studied in detail.

**Regime 3.**—In this regime, the transistor was kept at low drain voltage and fixed low gate voltage (in our case  $V_g = -1.5$  V,  $V_d = 0.2$  V) and the current transients were measured after the application of the higher drain voltage step of 3 V (thus studying the charge capture processes by traps induced by drain current flow).

Under these conditions the trapping caused by the flowing of the drain current after the  $V_d$  step 0.2 V  $\rightarrow$  3 V application resulted in a slow decrease of the drain current with time. Respective waveforms are shown for several temperatures in Fig. 5a. The drain current derivatives at each temperature could be represented by two peaks, a wide peak with low amplitude and a narrow peak with high amplitude. The waveforms of relaxations and of derivatives could be accurately approximated by the sum of two stretched exponents of the form  $A \exp[-(t/\tau)^\beta]$ .<sup>24</sup> Fig. 5b shows the results of fitting for one of the temperatures. The temperature dependences of  $\tau$  for respective extended exponents are depicted in Fig. 5c. For the main charge trapping process produced by application of high  $V_d$ , TP1d, the deduced activation energy was 1.1 eV. For the minor trapping process TP2d the temperature dependence of the relaxation time  $\tau$  was virtually absent.

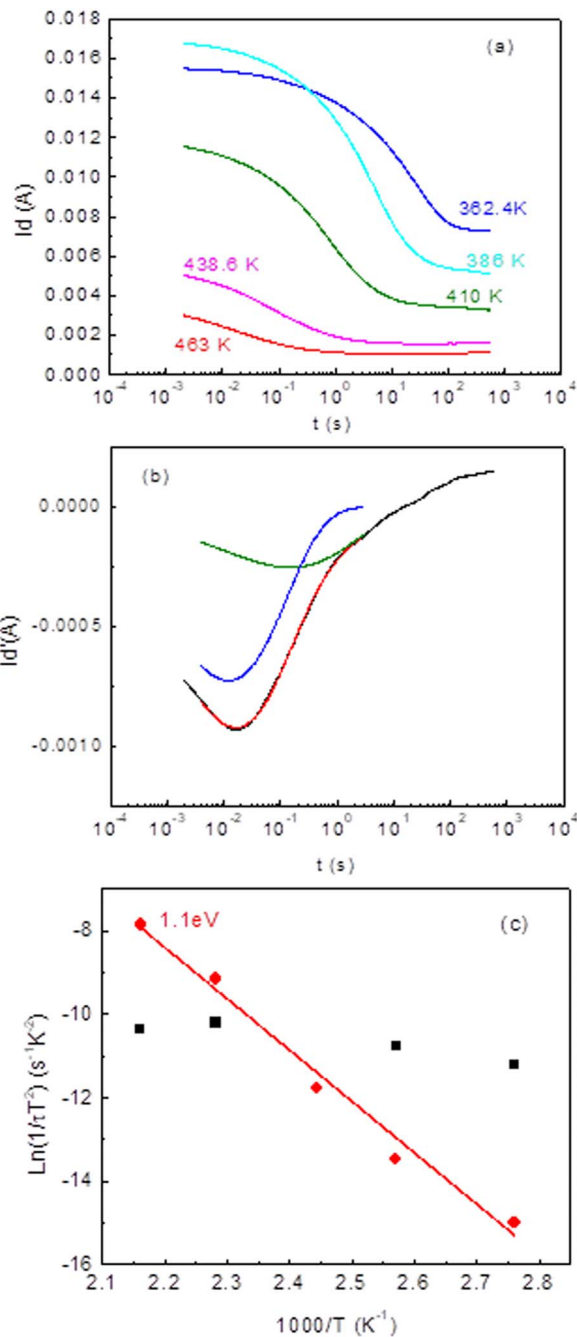


**Figure 4.** (a) CDLTS spectra of the InAlN/GaN HEMT taken at  $V_g = -0$  V,  $V_d = 0.1$  V,  $V_g$  pulse from 0 V to  $-9$  V with pulse lengths  $t_p$  of 0.1 s (magenta line), 0.5 s (blue line), 5 s (red line); (b) the dependence of the CDLTS peak amplitude on the pulse length; (c) the influence of the drain voltage  $V_d$  on measured CDLTS spectra.

In both processes the broadening constant  $\beta$  was much lower than 1 ( $\beta = 1$  corresponds to proper exponential decay.<sup>23,24</sup>)

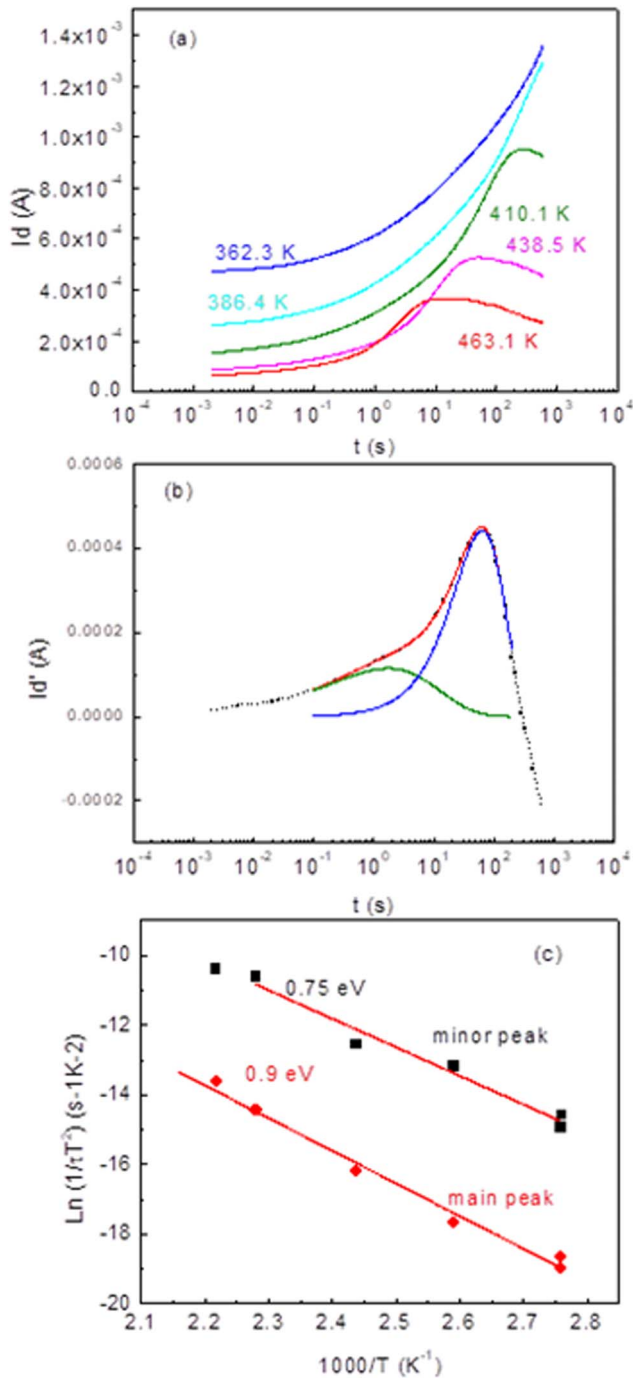
*Regime 4.*—This regime involved the step-wise transition of  $V_d$  from quiescent value of  $V_d = 3$  V to  $V_d = 0.2$  V at  $V_g = -1.5$  V (studying the detrapping caused by changes in the drain voltage).

The behavior in this regime is illustrated in Fig. 6a, 6b, 6c. The dominant feature is the drain current increase with time following the drain voltage 3 V  $\rightarrow$  0.2 V step (Fig. 6a). The drain current relaxations



**Figure 5.** (a) Drain current relaxations following the drain voltage step 0.2 V  $\rightarrow$  3 V at  $V_g = -1.5$  V; several relaxation curves are shown for measurement temperatures indicated near respective curves; (b) drain current derivative by logarithm of time for measurement temperature of 462.8 K (black curve) the blue curve is the result for the main peak represented as a stretched exponent with  $\beta = 0.45$ ,  $\tau = 0.0125$  s, the wide olive curve is the peak due to the stretched exponent with  $\beta = 0.35$ ,  $\tau = 0.185$  s, the red line is the sum of these two peaks; (c) the temperature dependence of  $\ln(1/\tau T^2)$  calculated by fitting experimental data for the main peak (solid circles) and the wide minor peak (solid squares).

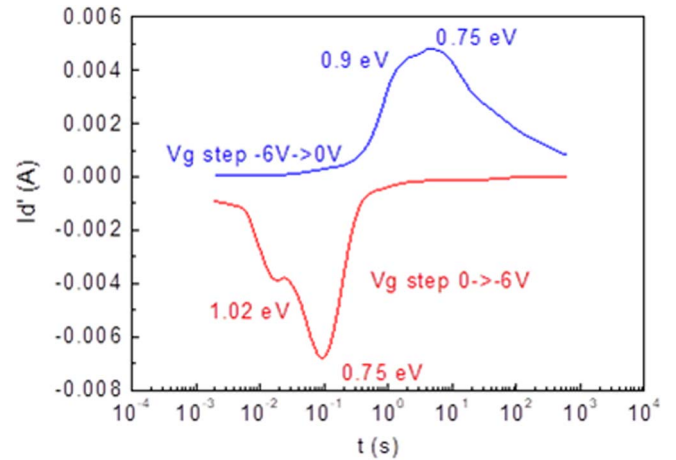
and the drain current derivatives could be accurately represented by superposition of two peaks corresponding to two stretched exponents (an example of the fitting of drain current derivative is given for one of the temperatures in Fig. 6b). The broadening factor for the major detrapping process DPd1 was close to 1 (the process is virtually purely exponential), the second process DPd2 was strongly nonexponential, with  $\beta$  much lower than unity. The temperature dependence of the



**Figure 6.** (a) Drain current relaxation curves following the drain voltage step from 3 V to 0.2 V at  $V_g = -1.5$  V; the data are shown for several temperatures indicated near respective relaxation curves; (b) representation of the drain current derivative by the sum of two stretched exponentials at  $T = 410.1$  K; the main relaxation (blue line) has  $\beta = 1$  and  $\tau = 61.7$  s, the minor relaxation has  $\beta = 0.44$ ,  $\tau = 1.75$  s (olive line), the red line is the sum of the two stretched exponentials, black line is the experimental data; (d) Arrhenius curves of  $\ln(1/\tau T^2)$  versus  $1000/T$  showing the derived activation energies for the main peak and the minor peak.

relaxation time for the major detrapping process DPd1 was 0.9 eV, for the minor process DPd2 it was 0.7 eV (Fig. 6d).

We also performed current relaxation measurements while applying gate voltage steps from 0 V to  $-6$  V at  $V_d = 0.5$  V and gate voltage steps from  $-6$  V to 0 V. The former regime mainly causes charge trapping under the gate, while the latter regime is associated with charge detrapping under the gate (the processes involved are believed to be



**Figure 7.** Drain current derivatives for gate voltage steps from 0 V to  $-6$  V (trapping processes TP1g and TP2g; red curve) and from  $-6$  V to 0 V (detrapping processes DP1g and DP2g, blue curve), both measurements done at  $V_d = 0.5$  V; the current derivatives are shown for  $T = 414.2$  K, the activation energies shown in the figure were obtained from drain current relaxation curves fittings by two stretched exponentials for various measurement temperatures.

similar to TP (CDLTS) and DP (CDLTS) processes in CDLTS (the gate voltage of  $-6$  V was chosen in these experiments as close to the threshold voltage at measurement temperatures in the range 350–450 K, as follows from Fig. 2). Fig. 7 shows the drain current derivatives calculated for the two gate voltage steps processes studied at 410.2 K. In both cases, two distinct peaks related to two stretched exponentials in the drain current relaxation curves were observed. Measurements at various temperatures in the range 350 K–450 K gave the activation energies of the trapping and detrapping processes indicated near respective relaxation curves in Fig. 7. Table I summarizes the information on various trapping and detrapping process observed in our experiments under various conditions.

## Discussion

Static and pulsed drain I-V characteristics in Fig. 1 indicate that both gate voltage pulsing and drain voltage pulsing seriously affect I-V characteristics, and the amount of drain current collapse can reach up to 25%, indicating a relatively strong trapping. Changes of the threshold voltage with temperature in transfer characteristics of HEMT in Fig. 2 point to a considerable role of deep traps under the gate whose net negative charge increases with temperature. CDLTS measurements in Figs. 3, 4 show that application of high gate voltage increases the net negative charge under the gate (or moves the negative charge closer to the InAlN interface) and this process (TP(CDLTS) in Table I) is temperature activated, with activation energy of 0.7–0.75 eV when assuming that the current transient is purely exponential.

The reverse process in CDLTS (gate pulsing from  $-9$  V to 0 or low negative values) indicates the decrease with time of the built-in negative charge under the gate during the pulse negative charge or movement of the charge farther from the interface. The activation energy of this DP(CDLTS) process is 1.05 eV if one assumes that the current transients are pure exponents. Increasing the drain voltage during these measurements causes additional charge trapping after the end of the gate pulse. The amplitude of CDLTS peaks in both processes depends logarithmically on pulse length, suggesting that traps along dislocation lines are involved.<sup>14,16,25</sup>

Drain current transient measurements after the application of 0.2 V to 3 V or 3 V to 0.2 V drain voltage steps at low gate voltages show that the flow of high drain current causes strong negative charge buildup and a decrease of the drain current with time. The relaxation curves are well described by a sum of two stretched exponentials. The

**Table I. Characteristics of trapping and detrapping processes observed after step-wise changes of the drain voltage and the gate voltage and processes observed in CDLTS upon gate voltage pulsing.**

Trap label	Observation conditions	$E_a$ (eV)
TP1d	V <sub>d</sub> step 0.2 V→3 V, V <sub>g</sub> = -1.5 V	1-1.1
TP2d	Same	~0
DP1d	V <sub>d</sub> step 3 V→0.2 V, V <sub>g</sub> = -1.5 V	0.9
DP2d	Same	0.75
TP1g	V <sub>g</sub> step 0→-6 V, V <sub>d</sub> = 0.5 V	0.75
TP2g	Same	1.05
DP1g	V <sub>g</sub> step -6 V→0 V	0.75
DP2g	V <sub>g</sub> step -6 V→0 V	0.9
TP(CDLTS)	CDLTS V <sub>g</sub> pulse -9 V→0 V, V <sub>g</sub> bias -9 V, V <sub>d</sub> = 0.5 V	0.7-0.75
DP(CDLTS)	V <sub>g</sub> pulse 0 V→-9 V, V <sub>g</sub> bias 0 V, V <sub>d</sub> = 0.5 V	1-1.1

main process of charge capture related to the high drain current flow (TP1d in Table I) is temperature activated with activation energy of 1.1 eV. The minor process (TP2d) is not temperature activated. The drain current recovery in the reverse process observed after the drain voltage switching from 3 V to 0.2 V is again accurately described by the sum of two stretched exponents, the major detrapping process DP1d having activation energy of 0.9 eV, the minor process DP2d an activation energy of 0.75 eV. According to the literature,<sup>17,25,27</sup> the temperature activated charge capture caused by high drain current flow is most likely due to traps between the gate and the drain, inducing the virtual gate extension.<sup>17,25,27</sup> The nature of the barrier for capture in the drain-current-driven processes requires further understanding. The activation energy is low, as for process TP2d in Table I, and is attributed to capture of electrons by traps in the GaN buffer.<sup>27</sup> The barrier for capture in the TP1d process could be associated with 2DEG electrons being excited into the InAlN barrier over the conduction band offset between InAlN and GaN (about 1.1 eV [1-4]). These electrons are then captured by some states in the barrier (near the interface because the injected electrons have to travel uphill against the electric field in the barrier). The reverse processes observed after the V<sub>d</sub> step from 3 V to 0.2 V should involve reemission of electrons captured at high drain voltage. Somewhat tentatively we assume that the major process DP1d is reverse to the major capture process TP1. The detrapping energies determined for the two processes DP1d and DP2d, 0.9 eV and 0.75 eV, could be related to respective energy levels in the barrier and in the buffer. However, additional studies on variously grown InAlN/GaN HEMTs are necessary for verification.

Gate voltage steps usually cause trapping-detrapping of electrons by states below the gate.<sup>17,25,27</sup> Such centers can be located in the barrier, near the interface or in the buffer. The trapping processes occurring after the application of the gate voltage step from 0 to -6 V (TP1g and TP2g processes in Table I) are obviously temperature activated, with the activation energies of 1.05 eV and 0.75 eV. For detrapping processes (gate voltage steps from -6 V to 0 V) DPg1 and DPg2, the activation energies are 0.9 eV and 0.75 eV, similar to the activation energies of detrapping for centers observed in drain voltage step experiments. Fig. 7 presents the drain current derivatives at 410.2 K for both processes and gives the obtained activation energies. The activation energies deduced from CDLTS gate pulsing spectra are not far from one of the centers observed for gate voltage steps experiments, particularly given the fact that in CDLTS analysis, the nonexponential nature of relaxation curves is not taken into account and the relaxation times in pulsing and step-wise experiments usually differ.<sup>23,24</sup> The real nature of the processes is not understood at the moment, but the logarithmic dependence of the magnitude of the TP(CDLTS) and DP(CDLTS) peaks magnitudes on the pulse length strongly suggests that the traps participating in gate voltage trapping and detrapping could be associated with dislocations. Centers similar to the (1-1.1) eV traps have been previously reported in CDLTS<sup>17</sup> as gate traps

determining the threshold voltage changes, while traps similar to our 0.75 eV traps have been observed in drain current relaxations induced by gate voltage steps.<sup>16</sup>

## Conclusions

Drain current transient analyses for gate voltage and drain voltage steps causing charge trapping and detrapping in our low-leakage current InAlN/GaN HEMTsshow that, in all cases studied, the current transients can be accurately described by a sum of two stretched exponents. For drain voltage steps from 0.2 V to 3 V causing electron trapping, the main trapping process is temperature activated, with activation energy of characteristic time of the stretched exponent ~1.1 eV. For the second minor trapping process, the characteristic relaxation time was virtually temperature independent. For drain voltage steps of 3 V to 0.2 V, the major detrapping process had activation energy of 0.9 eV, with a minor contribution from traps with activation energy of 0.75 eV. Since these trapping-detrapping processes were observed for low gate voltages far from the threshold voltage, the traps are believed to be located between the gate and the drain. The 1.1 eV activation energy of the trapping process is tentatively ascribed to 2DEG electron activation into the barrier traps whose energy level is located near 0.9 eV from the conduction band edge of the InAlN barrier as judged by the activation energy of the major detrapping process.

The gate voltage steps of 0 V to -6 V resulted in two trapping processes with activation energies 1.05 eV (major process) and 0.75 eV (minor process). Reverse gate voltage steps from -6 V to 0 V gave rise to two electron detrapping processes with activation energies 0.9 eV and 0.75 eV. Since the drain voltage in these experiments was low, the traps should be located under the gate and are believed to be responsible for threshold voltage decreases as the HEMT temperature was increased.

CDLTS spectra measured with gate current pulsing from -9 V to 0 V or from 0 V to -9 V revealed the presence of centers with activation energies of (0.7-0.75) eV and 1 eV similar to one of the traps observed in drain current transients produced by gate voltage steps. The magnitude of the CDLTS peaks in CDLTS logarithmically increased with the pulse length suggesting that these traps are associated with dislocations. CDLTS experiments can be used for rapid surveying of trapping and detrapping states in III-N based transistors, but have to be accompanied by detailed current relaxation transient analysis to better understand the details of the relaxation processes involved.

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