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Jihyun Kim, R. Mehandru, B. Luo, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, and Y. Irokawa

Characteristics of MgO/GaN gate-controlled metal–oxide–semiconductor diodes

Jihyun Kim, R. Mehandru, B. Luo, and F. Ren
Department of Chemical Engineering, University of Florida, Gainesville, Florida 32611

B. P. Gila, A. H. Onstine, C. R. Abernathy, and S. J. Pearton[a)]
Department of Material Science and Engineering, University of Florida, Gainesville, Florida 32611

Y. Irokawa
Toyoda Central Research and Development Lab, Inc., Nagakute, Aiche, 480-1192, Japan

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Gate-controlled n^+p metal–oxide–semiconductor diodes were fabricated in p-GaN using MgO as a gate dielectric and Si^+ implantation to create the n^+ regions. This structure overcomes the low minority carrier generation rate in GaN and allowed observation of clear inversion behavior in the dark at room temperature. By contrast, diodes without the n^+ regions to act as an external source of minority carriers did not show inversion even at measurement temperatures of 300 °C. The gated diodes showed the expected shape of the current–voltage characteristics, with clear regions corresponding to depletion and inversion under the gate. The MgO was deposited prior to the Si implantation and was stable during the activation annealing for the Si-implanted n^+ regions. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1487903]

There is great current interest in development of GaN-based metal–oxide–semiconductor (MOS) transistors because of their lower leakage currents and power consumption and capability for greater voltage swings relative to the more common Schottky-gate devices.[1–26] A wide variety of gate dielectrics for GaN have been reported, including oxides such as $Ga_2O_3(Gd_2O_3)$,[4,5,16,21,22] SiO_2,[2,6,8–12,17,18] MgO,[20] Sc_2O_3,[20] and insulators such as AlN[3,26] and SiN_x.[14,15,23] The deposition methods for these materials have included molecular beam epitaxy,[4,5,12,13,21,22] plasma-enhanced chemical vapor deposition,[8,18] photoelectrochemical oxidation,[19,24,25] and e-beam evaporation.[13,21,22] The interface state densities derived from the Terman method[27] are generally in the mid-to-high 10^{11} $eV^{-1}\,cm^{-2}$ range. Charge modulation from accumulation to depletion is commonly reported, but a clear demonstration of surface inversion has proven elusive due to the very low minority carrier generation rate in GaN at room temperature.[12] Even at 300 °C in conventional GaN MOS devices, the generation rate is still too low to observe inversion. To overcome a similar problem in SiC MOS devices, the n^+p junction of a MOS gate-controlled devices was employed as an external source of inversion charge.[28]

In this letter we report on the clear observation of inversion in MgO/p-GaN gate-controlled MOS diodes in which n^+ gated contact regions were created by Si^+ implantation and subsequent activation annealing with the MgO gate oxide in place. The frequency response of the diode capacitance–voltage ($C-V$) characteristic and the classical shape of the $I-V$ characteristic show the effectiveness of this approach in producing inversion at room temperature without external illumination.

The MgO was deposited by MBE at 100 °C on a p-GaN ($p\sim 3\times10^{17}$ cm^{-3} at 25 °C) layer grown by metalorganic chemical vapor deposition on sapphire. The MgO precursors were elemental Mg and radio-frequency plasma-activated oxygen. The GaN samples were cleaned initially with a 3 min chemical etch in HCl/H_2O (1:1), H_2O rinse, UV-ozone exposure for 25 min, rinsed in buffered oxide etch solution (6:1, NH_4F/HF), and rinsed in H_2O. The samples were then loaded into the MBE system and heated at 650 °C to ensure oxide removal. A standard effusion cell operating at 380 °C was used for evaporation of the Mg, while the O_2 source was operated at 300 W forward power (13.56 MHz) and 2.5×10^{-5} Torr. The MgO layers were ~800 Å thick. In separate measurements,[29] we obtained interface state densities of $2-3\times10^{11}$ $cm^2\,eV^{-1}$ from the ac conductance and Terman methods. For diode fabrication, implantation of 70, 195, and 380 keV $^{29}Si^+$ ions at a dose of 2×10^{13}, 6×10^{13}, 1.8×10^{14} cm^{-2}, followed by high temperature (~950 °C) activation annealing, was used to create the n^+ gate-contact regions. Following this step, the MgO was removed in all areas except for the gate, using H_3PO_4 etchant and an AZ-1045 resist mask. The e-beam deposited n-ohmic (Ti/Al/Pt/Au), p-ohmic (Pt/Au) contacts were followed by lift-off. A schematic of the final structure is shown in Fig. 1(top) and a scanning electron microscope (SEM) image is shown in Fig. 1(bottom).

Room temperature $C-V$ characteristics from a 40 μm diameter oxide contact MOS diode are shown in Fig. 2. We observe deep-depletion characteristics and no inversion behavior, even for measurement temperatures up to 300 °C (the limit of out test setup). In addition, the diode exhibited good rectification, demonstrating the MgO produces excellent insulator characteristics. The reverse breakdown of the diode with as-deposited dielectric was ~12 V, with a forward turn-on voltage of ~ 10 V. By sharp contrast, if the Pt/Au was placed directly on the p-GaN without any MgO, the forward turn-on voltage was <0.7 V and the reverse break-

a)Electronic mail: spear@mse.ufl.edu

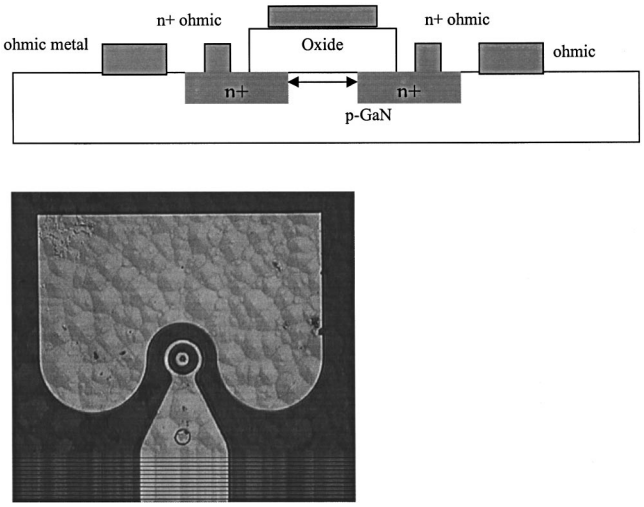

FIG. 1. Schematic cross-section of n^+p GaN MOS gate-controlled diode (top) and SEM plan view of device layout (bottom).

down voltage was <1 V. The forward breakdown field prior to annealing was ~ 1.2 MV cm^{-1} for the MgO, where we have defined breakdown as the voltage at which the forward current density is 5 mA cm^{-2}.

Figure 3 shows $C-V$ characteristics of the MgO/GaN MOS-controlled diodes at 25 °C in the dark as a function of the measurement frequency. In each case, -20 V was applied at the gated contact to provide a source of minority carriers. The frequency dispersion observed in inversion is due to the resistance of the inversion channel, as reported for n^+p SiC MOS gate-controlled diodes.[28] At 5 kHz measurement frequency, we observe only deep depletion since the characteristics are dominated by majority carriers.[30] As the frequency is decreased, a clear inversion behavior is observed due to charge flow into and from the n^+ regions external to the gate. It is likely that many of the gate oxides reported for GaN would also be capable of producing inversion behavior in MOS structures if a gated contact were included.[18,19,25] As mentioned earlier, in diodes without the n^+ regions to act as an external supply of minority carriers,

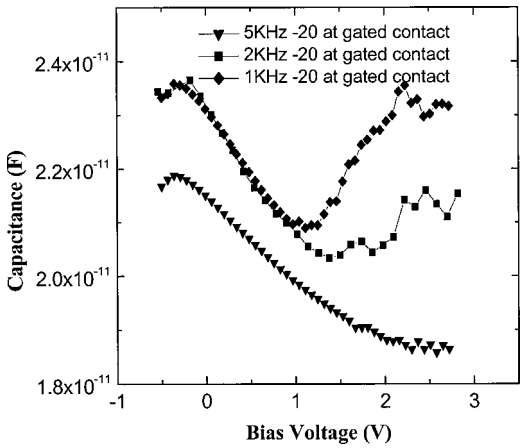

FIG. 3. $C-V$ characteristics of GaN MOS gate-controlled diodes at 25 °C as a function of measurement frequency (+15 V bias in gated contact in each case).

we could not observe inversion, even up to measurement temperatures of 300 °C.

Figure 4 shows $I-V$ characteristics from the diodes at 25 °C in the dark. For the accumulation region at negative bias, the reverse current is mainly due to diffusion and generation in the depletion region. As the bias is moved to positive values, the current increases due to the presence of two additional components, namely the additional depletion region under the gate provides more gate current and the surface generation current increases. As the bias is further increased to the inversion region, this surface generation component is suppressed, leaving only current due to generation in the depletion region. This is the classical behavior for a gate-controlled diode.[31]

In summary, we have demonstrated clear inversion in MgO/p-GaN MOS diodes at 25 °C in the dark by employing n^+ drain regions as a source of minority carriers. This provides a solution to the very low generation rate of minority carriers in GaN at room temperature. The MgO produces a relatively low interface state density on GaN and is stable against activation annealing for the implanted n^+ regions in the MOS gate-controlled diodes. This dielectric looks very

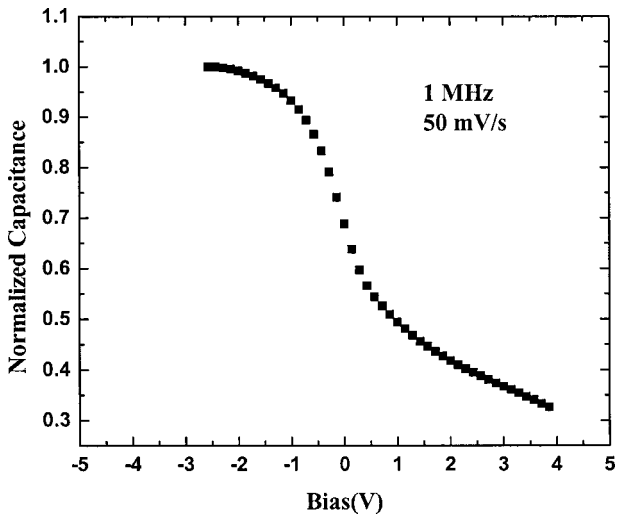

FIG. 2. 1 MHz $C-V$ characteristic at 25 °C of 40 μm diameter Pt/Au contact, conventional MgO p-GaN diode without any n^+ region to act a source of minority carriers.

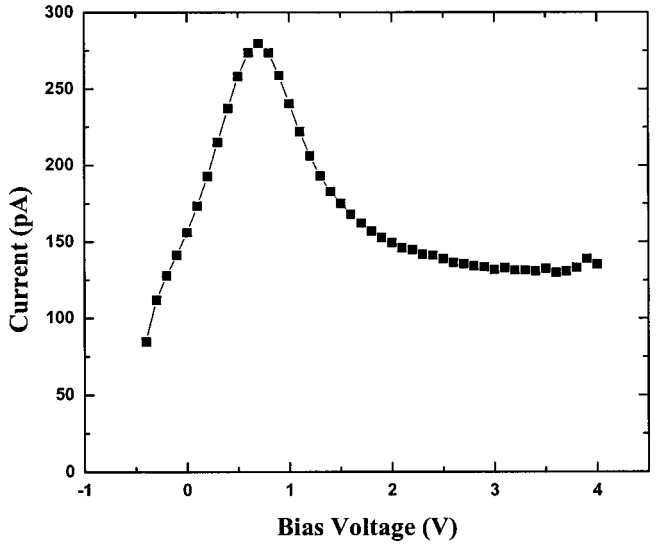

FIG. 4. $I-V$ characteristics of GaN MOS gate-controlled diodes at 25 °C, showing regions due to inversion (bias >2 V) and depletion (bias ~ 0.75 V).

promising for realization of enhanced-mode GaN MOS transistors.

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